CLAIMS

What is claimed is:

1. A method for forming a dual damascene structure in a semiconductor device manufacturing process comprising the steps of:

providing a process wafer comprising a via opening extending through at least one dielectric insulating layer;

blanket depositing a first photoresist layer to include filling the via opening;

blanket depositing a second photoresist layer over and contacting the negative photoresist layer;

photolithographically patterning the positive photoresist layer to form a trench opening etching pattern overlying and encompassing the via opening;

etching back the negative photoresist layer to form a via plug having a predetermined thickness partially filling the via opening; and,

etching a trench opening according to the trench opening etching pattern.

2. The method of claim 1, further comprising carrying out a plasma ashing process to remove remaining portions of the negative photoresist layer and the positive photoresist layer.

3. The method of claim 1, wherein the steps of etching back and etching a trench opening are carried out in-situ according to a plasma assisted etching process.

4. The method of claim 1, wherein the at least one dielectric insulating layer comprises a lower dielectric insulating layer and an upper dielectric insulating layer separated by a middle etch stop layer.

5. The method of claim 1, wherein the via plug is formed to fill the via opening to a level at about where a bottom portion of the trench opening is formed.

6. The method of claim 1, wherein an uppermost dielectric layer of the at least one dielectric insulating layer is provided with at least one of an overlying bottom anti-reflective coating (BARC) layer and an etch stop layer.

7. The method of claim 6, wherein the BARC layer comprises at least an inorganic layer selected from the group consisting of silicon oxynitride, silicon oxycarbide, and titanium nitride.

8. The method of claim 6, wherein the BARC layer is etched through to expose the at least one dielectric insulating layer during the step of etching back.

9. The method of claim 1, further comprising the step of at least one a photo-curing and a thermal curing process to harden the negative photoresist according to polymeric cross-linking reactions following the step of blanket depositing a negative photoresist layer.

10. The method of claim 9, wherein the negative photoresist is cured in a nitrogen containing ambient.

11. The method of claim 1, wherein the at least one dielectric insulating layer comprises a low-K dielectric insulating layer selected from the group consisting of fluorine doped silicon oxide, carbon doped silicon oxide, and organo-silane glass.

12. A method for forming a dual damascene structure in a semiconductor device manufacturing process comprising the steps of:

providing a process wafer comprising a via opening extending through at least one dielectric insulating layer and an uppermost bottom anti-reflective coating (BARC) layer;

blanket depositing a flowable negative photoresist layer to include filling the via opening;

curing the flowable negative photoresist layer according to at least a photo-curing process;

blanket depositing a positive photoresist layer over and contacting the negative photoresist layer;

photolithographically patterning the positive photoresist layer to form a trench opening etching pattern overlying and encompassing the via opening;

plasma etching back the negative photoresist layer to form a via plug having a predetermined thickness partially filling the via opening;

plasma etching in-situ with respect to the step of etching back a trench opening according to the trench opening etching pattern; and,

carrying out a plasma ashing process to remove remaining portions of the via plug and the positive photoresist layer.

13. The method of claim 12, wherein the at least one dielectric insulating layer comprises a lower dielectric insulating layer and an upper dielectric insulating layer separated by a middle etch stop layer.

14. The method of claim 12, wherein the via plug is formed to fill the via opening to a level at about where a bottom portion of the trench opening is formed.

15. The method of claim 12, wherein an uppermost dielectric layer of the at least one dielectric insulating layer is provided with at least one of an overlying bottom anti-reflective coating (BARC) layer and an etch stop layer.

16. The method of claim 12, wherein the BARC layer comprises at least an inorganic layer selected from the group consisting of silicon oxynitride, silicon oxycarbide, and titanium nitride.

17. The method of claim 12, wherein the BARC layer is etched through to expose the at least one dielectric insulating layer during the step of etching back.

18. The method of claim 12, wherein step of curing is carried out in a nitrogen containing ambient.

19. The method of claim 12, wherein the at least one dielectric insulating layer comprises a low-K dielectric insulating layer selected from the group consisting of fluorine doped silicon oxide, carbon doped silicon oxide, and organo-silane glass.

20. The method of claim 12, wherein the step of curing further comprises a thermal curing process to harden the negative photoresist.